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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. Claims 20-28 have been withdrawn; claims 1, 8-10, 12-13, 15-16, 18-19 and 29 have been amended herein to further emphasize various aspects of the invention.

1. (Currently amended) A system for monitoring and regulating a development process, comprising:
 - at least one development component operative to adapt one or more development parameters associated with developing a photoresist on at least one portion of a wafer;
 - a development component driving system for driving the at least one development component;
 - a system for directing light toward one or more gratings located on at least one portion of the wafer;
 - a development monitoring system operable to measure development progress from light reflected from the one or more gratings; and
 - a processor operatively coupled to the development monitoring system and the development component driving system, wherein the processor receives a development progress data from the measuring system and analyzes the development progress data by comparing the development progress data to stored development data to generate a feed-forward control data operative to control the at least one development component.
2. (Original) The system of claim 1, the development monitoring system further comprising a scatterometry system for processing the light reflected from the one or more gratings.
3. (Original) The system of claim 2, the processor being operatively coupled to the scatterometry system, the processor analyzing data received from the scatterometry system and producing an analyzed data and the processor controlling, at least in part, the at least one development component via the development component driving system based, at least in part, on the analyzed data.

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4. (Original) The system of claim 1, the development monitoring system further comprising a reflectometry system for processing the light reflected from the one or more gratings.
5. (Original) The system of claim 4, the processor being operatively coupled to the reflectometry system, the processor analyzing data received from the reflectometry system and producing an analyzed data and the processor controlling, at least in part, the at least one development component via the development component driving system based, at least in part, on the analyzed data.
6. (Original) The system of claim 3, the development monitoring system further comprising a reflectometry system for processing the light reflected from the one or more gratings.
7. (Original) The system of claim 6, the processor being operatively coupled to the reflectometry system, the processor analyzing data received from the reflectometry system and producing an analyzed data and the processor controlling, at least in part, the at least one development component via the development component driving system based, at least in part, on the analyzed data.
8. (Currently amended) The system of claim 3, ~~wherein~~ the scatterometry system is operable to detect a development end point and where the feed-forward control data is employed to terminate development.
9. (Currently amended) The system of claim 5, ~~wherein~~ the reflectometry system is operable to detect a development end point and where the feed-forward control data is employed to terminate development.
10. (Currently amended) The system of claim 7, ~~wherein~~ the scatterometry system is operable to detect a development end point, where the reflectometry system is operable to detect a development end point and where the feed-forward control data is employed to terminate development.

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11. (Original) The system of claim 8, the processor logically mapping the wafer into one or more grid blocks and making a determination of the acceptability of a development value in the one or more grid blocks.
12. (Currently amended) The system of claim 11, wherein the processor determines the existence of an unacceptable development value for at least a portion of the wafer based on comparing one or more measured development values to one or more stored development values.
13. (Currently amended) The system of claim 12, wherein the processor employs a non-linear training system in computing feed-forward control data operable to adjust the at least one development component.
14. (Original) The system of claim 9, the processor logically mapping the wafer into one or more grid blocks and making a determination of the acceptability of a development value in the one or more grid blocks.
15. (Currently amended) The system of claim 14, wherein the processor determines the existence of an unacceptable development value for at least a portion of the wafer based on comparing one or more measured development values to one or more stored development values.
16. (Currently amended) The system of claim 15, wherein the processor employs a non-linear training system in computing feed-forward control data operable to adjust the at least one development component.
17. (Original) The system of claim 10, the processor logically mapping the wafer into one or more grid blocks and making a determination of the acceptability of a development value in the one or more grid blocks.

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18. (Currently amended) The system of claim 17, wherein the processor determines the existence of an unacceptable development value for at least a portion of the wafer based on comparing one or more measured development values to one or more stored development values.

19. (Currently amended) The system of claim 18, wherein the processor employs a non-linear training system in computing feed-forward control data operable to adjust the at least one development component.

20-28. (Withdrawn)

29. (Currently amended) A system for monitoring and regulating a development process, comprising:
means for partitioning a wafer into one or more grid blocks;
means for sensing the acceptability of development in at least one of the one or more grid blocks utilizing light reflected from one or more gratings;
means for controlling the development of a wafer portion; and
means for selectively controlling the means for development.

30. (Original) The system of claim 29 where the means for controlling the development of a wafer portion comprise means for terminating the development process.